CLAIM LISTING:

1. (Withdrawn from Consideration) A method for providing data, said method comprising:

receiving a command from a node to provide data starting from an address;

providing data starting from the address and ending at a first address;

receiving an indication that the node can receive additional data; and

providing data starting from the first address and ending at a second address after receiving the indication.

2. (Withdrawn from Consideration) The method of claim 1, wherein the command is accompanied by a control signal indicating a particular mode of operation.

3. (Withdrawn from Consideration) The method of claim 1, further comprising:

storing the starting address.

4. (Withdrawn from Consideration) The method of claim 3, further comprising:

incrementing the starting address to equal the ending address.

5. (Currently Amended) A method for providing video data to a video decoder, said method comprising:

receiving a first request for a first macroblock row;

receiving a second request for a second macroblock row;

providing successive portions of the first macroblock row after receiving the first request and an indication that the video decoder has decoded a previous portion of the first macroblock row; and

providing successive portions of the second macroblock row after receiving the second request and an indication that the video decoder has decoded a previous portion of the second macroblock row, while providing successive portions of the first macroblock row, wherein the first request is accompanied by a starting address for the first macroblock row, and the second request is accompanied by a starting address for the second macroblock row, the method further comprising:

storing the first address; and

storing the second address.

6. (Cancelled)

7. (Currently Amended) The method of claim 5 ~~6~~, wherein providing successive portions of the first macroblock row further comprises:

incrementing the first starting address to a first intermediate address after providing a first of the successive portions of the first macroblock row; and

incrementing the second starting address to a second intermediate address after providing a first of the successive portions of the second macroblock row.

8. (Original) The method of claim 7, wherein providing successive portions of the first macroblock row, further comprises:

providing a portion from the first macroblock row that begins at the first intermediate address, after incrementing the first starting address to the first intermediate address.

9. (Original) A video decoder for decoding video data, said video decoder comprising:

a local buffer for storing a portion of the video data;

a decompression engine for decoding the portion of the video data stored in the local buffer; and

an extractor for transmitting an indicator to a direct memory access engine indicating that the local buffer can store another portion of the video data, after the decompression engine decodes the portions of the video data stored in the local buffer.

10. (Original) The video decoder of claim 9, wherein the decompression engine transmits a command to the direct memory access engine.

11. (Original) The video decoder of claim 9, wherein the local buffer stores another portion of the video data after the extractor transmits the signal to the direct memory access engine.

12. (Original) The video decoder of claim 9, further comprising:

a second local buffer for storing a second portion of the video data while the first local buffer stores the portion of the video data; and

a second extractor for transmitting an indicator to a direct memory access engine indicating that the second local buffer can store another portion of the video data, after the decompression engine decodes the second portion of the video data stored in the second local buffer.

13. (Withdrawn from Consideration) A direct memory access engine for providing data, the direct memory access engine comprising state logic that is operable to:

receive a command from a node to provide data starting from an address;

provide data starting from the address and ending at a first address;

receive an indication that the node can receive additional data; and

provide data starting from the first address and ending at a second address after receiving the indication.

14. (Withdrawn from Consideration) The direct memory access engine of claim 13 further comprising:

a register for storing the starting address.

15. (Withdrawn from Consideration) The direct memory access engine of claim 14, wherein the state logic machine is operable to increment the starting address to equal the ending address.

16. (Original) A direct memory access engine for providing video data to a video decoder, said direct memory access engine comprising state logic that is operable to:

receive a first request for a first macroblock row;

receive a second request for a second macroblock;

provide successive portions of the first macroblock row after receiving the first request and an indication that the video decoder has decoded a previous portion of the first macroblock row; and

provide successive portions of the second macroblock row after receiving the second request and an indication that the video decoder has decoded a previous portion of the second macroblock row, while providing successive portions of the first macroblock row.

17. (Original) The direct memory access engine 16, wherein the first request is accompanied by a starting address for the first macroblock row, and the second request is accompanied by a starting address for the second macroblock row, the direct memory access engine further comprising:

a first register for storing the first address; and

a second register for storing the second address.

18. (Original) The direct memory access engine of claim 17, wherein the state logic is operable to increment the first starting address to a first intermediate address after providing a first of the successive portions of the first macroblock row and increment the second starting address to a second intermediate address after providing a first of the successive portions of the second macroblock row.

19. (Original) The direct memory access engine of claim 18 wherein the state logic provides a portion from the first macroblock row that begins at the first intermediate address, after incrementing the first starting address to the first intermediate address.

20. (Original) A decoder system for decoding video data, said decoder system comprising:

a video decoder for decoding portions of the video data, said video decoder comprising:

a local buffer for storing the portions of the video data; and

an extractor for transmitting a signal indicating that a portion of the local buffer is available to store another portion of the video data; and

a direct memory access engine for providing the another portion of the video data to the portion of the local buffer, after receiving the signal from the extractor.